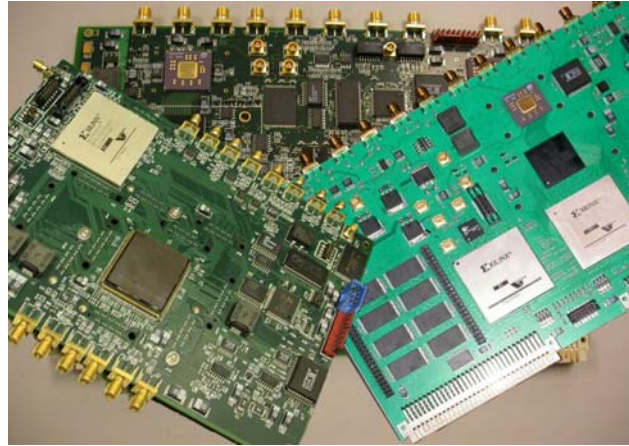


**LNX Corporation**  
8B Industrial Way  
Salem, NH 03079

## **LNX DUAL CHANNEL DIGITAL RECEIVER**

### **Introduction**

LNX has developed a dual channel, very high speed data acquisition and real-time Digital Signal Processing module. The board incorporates two Atmel TS83102, 2 Gsa/sec, 10-bit analog to digital converters and up to three Virtex-II Field Programmable Gate Arrays (FPGAs); the board also has two high-speed serial (Hotlink) interfaces and a VME64 interface. Typical applications include Electronic Warfare, radar, and software defined radios.



**Figure 1 LNX 's Digital Products, Including Single and Dual Channel Digital Receivers.**

### **Item Description**

#### *A/D*

The board incorporates two TS83102 A/Ds from Atmel. This device has a maximum sample rate of 2 Gsa/sec at 10-bits with a 3 GHz full power input bandwidth. Spurious free dynamic range is 58 dBc (7.4 effective bits at  $F_S = 1.4$  Gsa/sec,  $f_{IN} = 700$  MHz). A companion device, the TS81102 demultiplexes the high speed, 10-bit ECL A/D outputs onto an 80-bit, single-ended bus running at 1/8 of the sample rate. The A/D's sampling delay and gain can be adjusted to support synchronizing and interleaving multiple A/D boards. The output of the demultiplexer is connected to a Virtex-II FPGA using an 80-bit single-ended data bus and a differential clock.

#### *FPGAs*

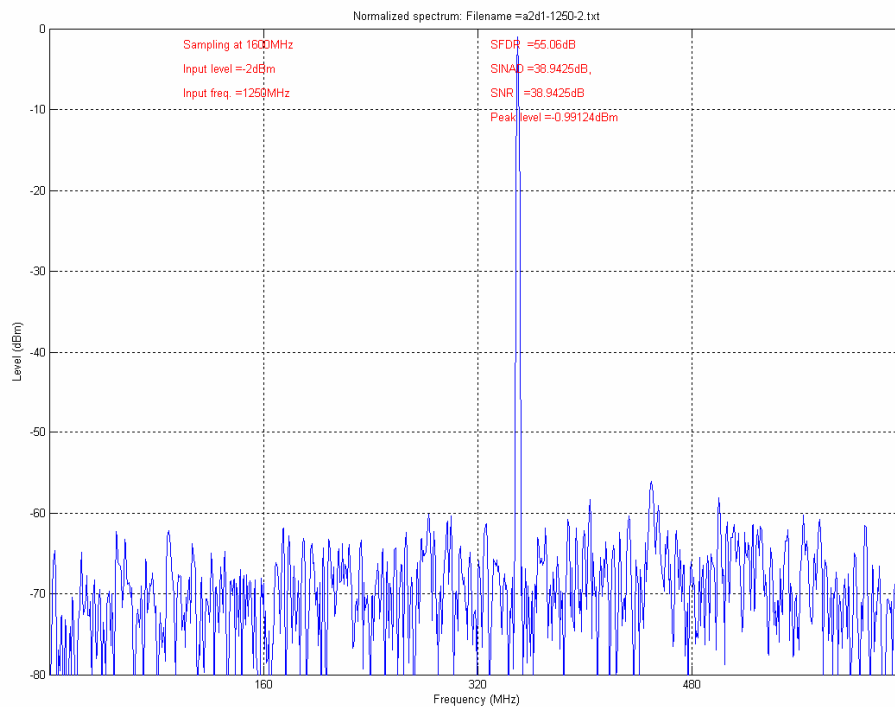
There are sites for three Virtex-II FPGAs; each site can support devices ranging from 2 to 8 million gates. The FPGAs are also used to implement the Hotlink and VME interfaces. Two devices also have a CPU bus for direct communication with an on-board CPU.

## CPU

An on-board CPU module is used to provide a user interface, local control, and FPGA configuration. This module also provides an RS232 interface. There are 32 megabytes of Flash memory that can be used to store FPGA configuration data. A simple command set is used to configure and control data collection and processing.

## Hotlink Interface

High speed serial links are implemented using the CYP15G0101DXA HOTLink II™ Transceiver from Cypress Semiconductor. It contains all of the logic to support the serialize/de-serialize (SERDES) function and clock recovery and supports data rates from 200-1500 Mbaud.



**Figure 2 Direct downconversion of 1250 MHz signal, sampled at 1600 Gsa/sec. Spurious free dynamic range exceeds 55 dB.**

### *VME Interface*

The VMEbus interface is designed to conform to the VME64x specification and requires the 160 pin connectors with the added ground pins and +3.3 volt power pins. The interface was designed to support A32/D32 slave data transfer.

### *Power*

Power can be supplied through a 10-pin terminal block for bench top operation or the VME backplane. The special power supply voltages, that are not part of the VME specification, are supplied through user defined pins. Typical power consumption is 60W.

### *Additional Capabilities*

LNX can develop custom algorithms based on customer specifications. LNX has made a significant investment in system simulation, algorithm development, and FPGA logic synthesis tools. Our tools allow us to develop and simulate fixed-point DSP algorithms in Matlab™ and automatically convert those algorithms into VHDL for synthesis and implementation on the FPGAs. This allows us to rapidly develop, simulate, and test new algorithms without having to manually convert new algorithms to VHDL or Verilog.

### **Conclusion**

LNX has developed a very high speed data acquisition and real-time DSP processing platform. With the tools and capabilities we have in house, we can easily tailor the design, using lower cost design techniques, as necessary to implement new requirements.